EXAMINER'S AMENDMENT AND REASONS FOR ALLOWANCE

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given by applicant's agent or attorney of record, John P. Wagner, via a telephonic examiner-initiated interview on 6/3/2009, wherein amendments to all independent claims were discussed. The purpose of the amendment is to clarify the invention and to distinguish the invention from the prior art of record.

The application has been amended as follows:

Please amend the claims as indicated in the complete listing of the claims attached to the end of this document. - See pages 7-9.

The following is the Examiner's statement of reasons for allowance:

The prior art of record does not disclose nor render obvious the claimed subject matter as recited in amended Claims 5-10 and 12-15 (to be renumbered claims 1-10 respectively), especially regarding amended independent Claim 5 (to be renumbered 1) and its limitations comprising:

Claim 5 (to be renumbered Claim 1):

"identifying a cycle during which an operation is available for a first functional unit and no operation is available for a second functional unit, wherein the first and second functional units comprise functional units of a same type;

scheduling the operation for execution by both the first and second functional units during the cycle;

scheduling a comparison of results obtained by the first and second functional units during a subsequent cycle;

wherein the method is performed by a scheduler in a code generator of a program compiler"

in the context of their remaining claim limitations and as best illustrated by figures 4 and 5 of the as-filed specification.

The closest prior art of record, Metzger (U.S. Patent Application No. 7,269,827), Tirumalai et al. (U. S. Patent Application No. 7,234,136) (hereinafter, "Tirumalai"), Raina (U.S. Patent Application No. 6,134,675), Quach (U. S. Patent Application No. 6,640,313), and Oh et al., "Error Detection by Duplicated Instructions in Super-Scalar Processors", IEEE, 2002 (hereinafter 'Oh'), do not separately anticipate nor jointly or in combination with other prior art disclosures render obvious the aforementioned limitations of the pending independent claims.

Regarding Tirumali, Quach, Raina and Metzger, Examiner agrees with Applicants' remarks comprsing:

Applicants respectfully submit that Tirumalai's method of generating multiple redundant prefetches to multiple functional units conflicts with Metzger's intended purpose of allocating unscheduled instructions to these multiple functional units, and therefore would render Metzger's unsatisfactory for its intended purpose. Furthermore, Metzger's method of allocating unscheduled instructions to multiple functional units conflicts with Tirumalai's intended purpose of filling "instruction slots ... with redundant prefetch operations" (Tirumalai, column 9, lines 10-12), and therefore would render Tirumalai unsatisfactory for its intended purpose. Metzger and Tirumalai have such different structures and different intended functions that the modification of each by the other would render both Metzger and Tirumalai unsatisfactory for each's intended purpose.

Furthermore, Applicants respectfully agree with the instant Office Action that states, "Metzger also does not disclose multiple functional units of a same type" (instant Office Action, page 4, section 2). However, the instant Office Action further states, "... Raina discloses multiple functional units of the same type" (instant Office Action, page 4, section 2). Applicants respectfully note that the Claim 1 features of "opportunistically scheduling a redundant operation on one of the functional units that would otherwise be idle during a cycle" is performed by a program compiler.

Applicants respectfully submit that the combination of Metzger, Tirumalai, and Quach as a whole fails to suggest the features of Applicants' Claim 1 because Tirumalai and Quach teach away from Applicants' Claim 1, the combination of Metzger and Tirumalai would render both Metzger and Tirumalai unsatisfactory for their intended purposes, and Raina should not be applied as described herein. Furthermore, Applicants respectfully submit that the instant Office Action fails to explain the differences between Applicants' Claim 1, Metzger, Tirumlai, Raina, and Quach.

(Remarks, pg. 12-14; emphasis original).

Oh discloses a method of error detection comprising duplicating instructions on idle functional units, analogously to the method of the amended claims. However, Oh does not disclose nor in combination with any other reference render obvious the method step of scheduling the duplicated instructions and subsequent comparison in a compiler. Therefore, the cited references, taken alone or in view of any other recorded reference, do not anticipate nor render obvious the invention of the amended independent claims, specifically regarding the aforementioned claim limitations. Accordingly, the pending claims are patentable over the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN D. COYER whose telephone number is (571) 270-5306, and whose fax number is (571) 270-6306.. The examiner can normally be reached via phone on Mon-Thurs, 9a-7p. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen, can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RYAN D COYER/
Examiner, Art Unit 2191

/Wei Y Zhen/
Supervisory Patent Examiner, Art Unit 2191

PLEASE AMEND THE CLAIMS AS FOLLOWS:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Currently Amended) A method of compiling a program to be executed on a target microprocessor, the method comprising:

determining whether a functional unit of the microprocessor would be idle at runtime;

identifying a cycle during which an operation is available for a first functional unit and no operation is available for a second functional unit, wherein the first and second functional units comprise functional units of a same type;

scheduling the operation for execution by both the first and second functional units during the cycle;

scheduling a comparison of results obtained by the first and second functional units during a subsequent cycle;

providing notification if the comparison indicates an error;

wherein the method is performed by a scheduler in a code generator of a program compiler.

6. (Original) The method of claim 5, wherein the first and second functional units comprise first and second floating point units of the target microprocessor.

7. (Original) The method of claim 5, wherein the first and second functional units comprise first and second arithmetic logic units of the target microprocessor.

8. (Original) The method of claim 5, wherein the results of the execution are stored in registers within the microprocessor, and the comparison of results compares contents of those registers.

9. (Original) The method of claim 5, wherein the target microprocessor includes at least three functional units of the same type.

10. (Original) The method of claim 9, further comprising:

identifying that during the cycle a second operation is available for a third functional unit of the same type and no operation is available for a fourth functional unit of the same type;

scheduling the second operation for execution by both the third and fourth functional units during the cycle; and

scheduling a comparison of results obtained by the third and fourth functional units during a subsequent cycle.

11. (Canceled)

12. (Currently Amended) The method of claim 5 ~~11~~, wherein the program compiler comprises a native complier for the target microprocessor.

13. (Currently Amended) The method of claim 5 ~~11~~, wherein the program compiler comprises a cross compiler run on a different microprocessor.

14. (Original) The method of claim 5, further comprising:

causing a flag to be set when the comparison indicates an error.

15. (Original) The method of claim 14, further comprising:
if the error flag is set, then halting the execution and causing a notification to the user of the error flag.

16. (Canceled)

17. (Canceled)

18. (Canceled)